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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/912,558	07/26/2001	Ronald A. Weimer	M4065.0319/P319-A	5990

24998 7590 05/08/2002

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EXAMINER

KIELIN, ERIK J

ART UNIT	PAPER NUMBER
2813	# 12

DATE MAILED: 05/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Offic Action Summary</b>	Application No.	Applicant(s)
	09/912,558	WEIMER ET AL.
Examiner	Art Unit	
Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 10 April 2002.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 13, 14, 16, 17, 41 and 42 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 13, 14, 16, 17, 41 and 42 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All
  - b) Some \*
  - c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
  - a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____.
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.	6) <input type="checkbox"/> Other: _____

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 13, 16-17, and 42 are rejected under 35 U.S.C. 102(a) as being anticipated by the article **Luan, et al.** “Ultra thin high quality Ta<sub>2</sub>O<sub>5</sub> gate dielectric prepared by in-situ rapid thermal processing” Electron Devices Meeting, held 6-9 December 1998, IEDM ‘98 Technical Digest, pp. 609-612.

Regarding independent claims 13, 41, and 42, **Luan** discloses a method of forming a gate dielectric layer on a substrate comprising the steps of

depositing a dielectric film over an active region of a semiconductor substrate to form part of a gate of a transistor, wherein the dielectric film is tantalum oxide (Ta<sub>2</sub>O<sub>5</sub>), as further limited in claim 17, having the inherent property of a dielectric constant of “at least about 25” (Introduction), as further limited in instant claim 16; and

subjecting the dielectric film to a wet oxidation using rapid thermal processing (RTP) and therefore occurring, by definition, in a RTP chamber, at a temperature of 600 °C for a period of about 40-50 seconds (Fig. 1) as further limited in instant claim 15, wherein the wet oxidation environment is formed by heating a mixture of H<sub>2</sub> and O<sub>2</sub>. (See whole **Luan** article which is very brief.)

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 14 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Luan** in view of US 6,063,698 (**Tseng** et al.).

The prior art, as explained above, teaches all of the features of the claims except for indicating a temperature in the range of 750-950 °C.

**Tseng** teaches a process virtually identical to **Luan** of forming a tantalum oxide gate dielectric 14 on a semiconductor substrate 12 and then wet oxidizing by heating a mixture of H<sub>2</sub> and O<sub>2</sub> to a temperatures of 750-850 °C to beneficially “eradicate trap sites 16 and 18” (col. 6, lines 39-57). (See also Abstract; col. 5, line 54 to col. 6, line.)

It would have been obvious to one of ordinary skill at the time of the invention to modify the method of **Luan** to use the temperature taught by **Tseng** in order to beneficially reduce the trap sites as taught by **Tseng**. --especially since the methods are virtually the same.

Regarding claim 41, if it is thought that **Luan** does not inherently teach an actual thickness of Ta<sub>2</sub>O<sub>5</sub> of greater than 40 Å, then this may be a difference. But **Tseng** teaches that a T<sub>eq</sub> (*equivalent* thickness relative to an actual thickness of SiO<sub>2</sub>) of 20 Å is equal to an actual thickness T<sub>actual</sub> of 60 Å of high dielectric constant material (e.g. tantalum oxide, Ta<sub>2</sub>O<sub>5</sub>). (See **Tseng**, col. 4, line 35-43). This indicates that the **Luan** T<sub>actual</sub> is **necessarily** thicker than the T<sub>eq</sub> reported because tantalum oxide is a high dielectric constant material. **Luan** teaches a T<sub>eq</sub> of 13-

25 Å wherein the 13 Å  $T_{eq}$  is the “thinnest ever reported.” (See Luan, first paragraph under the section entitled, “2. Leakage Current”)

Accordingly, it would be obvious for one of ordinary skill in the art, at the time of the invention, to form the tantalum oxide in Luan to  $T_{actual}$  60 Å to attain the  $T_{eq}$  of about 20 Å reported in Luan, as taught also by Tseng.

#### ***Response to Arguments***

Applicant's arguments filed 4/10/02 have been fully considered but they are not persuasive.

Applicant argues on p. 4, first paragraph regarding the Luan article,

“Luan does not teach or suggest the formation of a semiconductor device by ‘depositing a dielectric film over an active region of a semiconductor substrate to form *part of a gate of a transistor*’ and ‘subjecting the dielectric film to a *wet oxidation with steam* provided by heating a mixture of hydrogen and oxygen gases in a rapid thermal process chamber...’”  
(Emphasis original.)

This argument is wholly without merit. First, Luan is forming **gate dielectrics** for the **gate** of **MOSFETs**. (See Introduction.) Second, the MOS capacitor is merely used to **test the leakage current** of the **gate dielectric**, which is, nonetheless, for use as “*part of a gate of a transistor*” (emphasis original) as taught in Luan. Third, both Applicant and Luan heat mixtures of H<sub>2</sub> and O<sub>2</sub> to form water (H<sub>2</sub>O) in its vapor state --i.e. steam. If Luan is not forming steam then Applicant has a *major enablement problem* since both are heating mixtures of H<sub>2</sub> and O<sub>2</sub>, to temperatures greater than 450 °C, which necessarily produces steam. Applicant is requested to provide evidence that Luan is somehow **not** forming steam, but Applicant, with the same mixture

and the same temperature is somehow forming steam. (See Van Zant, Microchip Fabrication, 4<sup>th</sup> ed. McGraw-Hill: New York, 2000, pp. 172-173.) Accordingly, the arguments regarding the Luan article are wholly without merit.

Applicant's argument regarding the Luan article in view of Tseng is not persuasive. Luan would not abandon the extremely beneficial rapid thermal processing (RTP) simply because a different temperature (that in Tseng) is employed. As is notoriously well known to those of ordinary skill in the art, RTP reduces the thermal budget by reducing the time at a given temperature, and Tseng teaches that the temperature is beneficial for reducing traps, so one of ordinary skill would beneficially use the temperature in Tseng to reduce traps. Furthermore, the time at temperature is merely an obvious matter of routine optimization to achieve the desired result of the anneal process.

Applicant's arguments regarding claim 41 are moot in view of the new ground of rejection, necessitated by Applicant's amendment to claim 41.

### *Conclusion*

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,197,668 B1 (Gardner et al.) teaches a Ta<sub>2</sub>O<sub>5</sub> gate dielectric which is RTA processed after deposition in NH<sub>3</sub> at a temperature of 900-1100 °C. (See col. 3, lines 39-66.)

Lu et al. "Leakage current comparison between ultra-thin Ta<sub>2</sub>O<sub>5</sub> films and conventional gate dielectrics" IEEE Electron Device Letters 19(9), 9/1998, pp. 341-342 teaches a Ta<sub>2</sub>O<sub>5</sub> gate

dielectric which is RTA processed after deposition in NH<sub>3</sub> at a temperature of 800 °C for 30 seconds. (See Abstract and section entitled “Fabrication.”)

**Alers**, et al. “Intermixing at the tantalum oxide/silicon interface in gate dielectric structures” Applied Physics Letters 73(11), 14 September 1998, pp. 1517-1519 teaches a Ta<sub>2</sub>O<sub>5</sub> gate dielectric which is RTA processed after deposition in O<sub>2</sub> at a temperature of 800 °C. (See Abstract; Fig 1; p. 1519, first paragraph.)

US Patent Application Publication 2001/0020725 A1 (**Okuno** et al.) teaches a Ta<sub>2</sub>O<sub>5</sub> gate dielectric which is RTA processed after deposition in O<sub>2</sub> or N<sub>2</sub> at a temperature of 700 °C for 60 seconds. (See paragraph [0032].)

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication from examiner should be directed to Erik Kielin whose telephone number is (703) 306-5980 and e-mail address is [erik.kielin@uspto.gov](mailto:erik.kielin@uspto.gov). The examiner can normally be reached by telephone on Monday through Thursday 9:00 AM until 7:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached at (703) 306-2794 or by e-mail at [olik.chaudhuri@uspto.gov](mailto:olik.chaudhuri@uspto.gov). The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications..

EK

April 24, 2002



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